CLAIMS

1. A parallel pulse signal processing apparatus including a plurality of pulse output arithmetic elements, a plurality of connection elements which parallelly connect predetermined elements of the arithmetic elements, and a gate circuit which selectively passes pulse signals from the plurality of connection elements,

characterized in that said arithmetic element comprises

input means for inputting a plurality of time series pulse signals,

modulation processing means for executing predetermined modulation processing on the basis of the plurality of time series pulse signals which are input, and

pulse output means for outputting a pulse signal on the basis of a result of modulation processing, and

said gate circuit selectively passes, of the signals from said plurality of connection elements, a finite number of pulse signals corresponding to predetermined upper output levels.

2. The apparatus according to claim 1, characterized by further comprising a timing signal generation circuit to generate a predetermined timing signal,

wherein after the predetermined timing signal

from said timing signal generation circuit is input, said gate circuit selectively passes, of the signals from said plurality of connection elements, the finite number of pulse signals corresponding to the predetermined upper output levels.

3. The apparatus according to claim 2, characterized in that said gate circuit selectively passes, of the signals from said plurality of connection elements, the signals in ascending order of delays with respect to the timing signal from said timing signal generation circuit.

4. The apparatus according to claim 1, characterized in that said gate circuit is connected to a predetermined bus connected to said plurality of connection elements and selectively passes the finite number of pulse signals corresponding to the predetermined upper output levels from among the pulse signal propagating on the bus.

5. The apparatus according to claim 1, characterized in that said arithmetic element integrates an input pulse signal train in a predetermined time window and outputs the pulse signal at one of a phase and a frequency corresponding to the integration value.

6. The apparatus according to claim 1, characterized in that said gate circuit includes a switching circuit selectively connected to, of said plurality of connection elements, a connection element whose connection strength takes a maximum value and not less than a predetermined level.

7. A parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, characterized by comprising:

a plurality of arithmetic elements which receive signals from different layer levels and outputs predetermined pulse signals by a predetermined local receptor field structure; and

a gate circuit element which selectively passes the pulse signals from said plurality of arithmetic elements belonging to a predetermined receptor field in accordance with a signal level of the pulse signal.

8. A parallel pulse signal processing apparatus including input means for inputting data in a predetermined dimension, a plurality of data processing means, a gate circuit which selectively passes signals from said data processing means, and output means for outputting a result of pattern detection,

characterized in that said data processing means includes a plurality of arithmetic elements parallelly

connected by predetermined connection means,

said arithmetic element included in said data processing means outputs a pulse-shaped signal train representing a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window, and

said output means outputs the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements.

9. A parallel pulse signal processing apparatus including input means for inputting data in a predetermined dimension, a plurality of data processing means for outputting pulse signals, a gate circuit which selectively passes signals from said data processing means, and output means for outputting a result of pattern detection,

characterized in that said data processing means includes a plurality of arithmetic elements parallelly connected by predetermined connection means,

said gate circuit selectively passes the pulse signals on the basis of signal levels of the pulse signals from said plurality of data processing means,

said arithmetic elements receive a time series pulse signal, identify time series pulse signal

patterns of a plurality of classes, and output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window, and

said output means outputs the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements.

10. A parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, characterized by comprising:

input means for inputting one of an intermediate result of different layer levels and data from a predetermined memory;

a plurality of data processing means, having a feature detection layer which detects a plurality of features from the data input by said input means, for outputting pulse signals; and

a timing signal generation circuit,

said data processing means further comprising

a plurality of arithmetic elements which receive detection signals of the features of different types from a layer level of a preceding stage and output predetermined pulse signals, and

a gate circuit which selectively passes outputs from said arithmetic elements involved in the plurality of predetermined features,

wherein said arithmetic elements output pulse-shaped signals at one of a frequency and a timing based on a plurality of input signals from said timing signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window.

11. The apparatus according to claim 1, characterized in that said gate circuit includes a switching circuit selectively connected to, of said plurality of connection elements, a connection element whose connection strength has not less than a predetermined level.

12. The apparatus according to claim 1, characterized in that said gate circuit selectively passes, of the signals from said connection elements, the signals in ascending order of delays with respect to a predetermined reference time.

13. The apparatus according to claim 1, characterized in that said gate circuit selectively passes, of the plurality of pulse signals, the signals having a maximum output level.

14. The apparatus according to claim 1, characterized in that said gate circuit selectively passes, of the

signals from said connection elements, a predetermined number of signals having a maximum value from an uppermost level.

15. The apparatus according to claim 7, characterized in that said gate circuit selectively passes pulse signals corresponding to upper output levels for each feature.

16. A pattern recognition apparatus characterized by comprising a parallel pulse signal processing apparatus of claim 1.

17. An image input apparatus characterized in that pattern recognition is executed by using a parallel pulse signal processing apparatus of claim 1, and input control of a predetermined image signal is executed on the basis of the pattern recognition result.

18. A control method of a parallel pulse signal processing apparatus comprising a plurality of pulse output arithmetic elements, a plurality of connection elements which parallelly connect predetermined arithmetic elements, and a gate circuit which selectively passes pulse signals from the plurality of connection elements,

characterized in that the arithmetic element

inputs a plurality of time series pulse signals,

executes predetermined modulation processing on the basis of the plurality of time series pulse signals which are input, and

outputs a pulse signal on the basis of a result of modulation processing, and

the gate circuit selectively passes, of the signals from the plurality of connection elements, a finite number of pulse signals corresponding to predetermined upper output levels.

19. A control method of a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, characterized by comprising:

causing a plurality of arithmetic elements to receive signals from different layer levels and output predetermined pulse signals by a predetermined local receptor field structure; and

causing a gate circuit element to selectively pass the pulse signals from the plurality of arithmetic elements belonging to a predetermined receptor field in accordance with a signal level of the pulse signal.

20. A control method of a parallel pulse signal processing apparatus comprising input means for inputting data in a predetermined dimension, a

plurality of data processing means, a gate circuit which selectively passes signals from the data processing means, and output means for outputting a result of pattern detection,

characterized by comprising causing each of a plurality of arithmetic elements, which are included in the data processing means and parallelly connected by predetermined connection means, to output a pulse-shaped signal train representing a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window, and

causing the output means to output the detection result of the predetermined pattern in the data on the basis of the outputs from the arithmetic elements.

21. A control method of a parallel pulse signal processing apparatus comprising input means for inputting data in a predetermined dimension, a plurality of data processing means for outputting pulse signals, a gate circuit which selectively passes signals from the data processing means, and output means for outputting a result of pattern detection,

characterized by comprising causing the gate circuit to selectively pass the pulse signals on the basis of signal levels of the pulse signals from the

plurality of data processing means,

causing a plurality of arithmetic elements, which are included in the data processing means and parallelly connected by predetermined connection means, to receive a time series pulse signal, identify time series pulse signal patterns of a plurality of classes, and output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window, and

causing the output means to output the detection result of the predetermined pattern in the data on the basis of the outputs from the arithmetic elements.

22. A control method of a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations, the parallel pulse signal processing apparatus comprising input means for inputting one of an intermediate result of different layer levels and data from a predetermined memory, a plurality of data processing means, having a feature detection layer which detects a plurality of features from the data input by the input means, for outputting pulse signals, and a timing signal generation circuit,

characterized by comprising, under the control of the data processing means, causing a plurality of arithmetic elements to receive detection signals of the

features of different types from a layer level of a preceding stage and output predetermined pulse signals, and

causing a gate circuit element to selectively pass outputs from the arithmetic elements involved in the plurality of predetermined features, and

causing the arithmetic elements to output pulse-shaped signals at one of a frequency and a timing based on a plurality of input signals from the timing signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window.

23. A control method of a pattern recognition apparatus characterized by comprising a parallel pulse signal processing apparatus of claim 1.

24. A control method of an image input apparatus characterized by comprising executing pattern recognition by using a parallel pulse signal processing apparatus of claim 1, and executing input control of a predetermined image signal on the basis of the pattern recognition result.